BESS Inverters - Test specification

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The purpose of this document is to describe and define guidelines of the type tests for BESS Grid Forming (GFM) inverters to be connected to the HV/EHV grid in Israel under supervision of NOGA – Independent System Operator.

The inverter's manufacturer is required to prepare procedures for all the following test cases and provide them to NOGA, for approval before setting up the test bed.

Content

1. General

1. For each test case, the Inverter Manufacturer is required to elaborate and present the scheme of the required test bed, that will be constructed to demonstrate the test and the inverter's capabilities.
2. The manufacturer is required to elaborate the test steps to be performed for each test case.

2. Over /Under frequency protection (OF/UF)

The purpose of this test is to verify the protection levels and disconnection times of the inverter concerning over- and under-frequency.

The inverter will operate continuously in the frequency range between 47 Hz and 53 Hz (47<f<53).

Procedure (UF):

The frequency of the separate 3 phase voltage supply shall be decreased from 100 % of nominal frequency at nominal voltage in steps of 0.2 Hz until the inverter disconnects from the AC grid. Each step shall take at least 5 sec.

The value of the frequency that leads to the disconnection of the inverter, as well as the disconnection time, will be recorded and documented. The same procedure will be repeated for over-frequency (OF). During the tests the inverter will run at partial output power and nominal AC Voltage.

The measurements will be documented in the following table format:

	Protection Level		**Disconnection Time**	
	Setpoint	**Measured**	**Setpoint**	**Measured**
Over-frequency (OF)	53Hz		200ms	
Under-frequency (UF)	47 Hz		1000ms	

Table 1: Frequency disconnection settings

The use of a separate 3 phase voltage supply, which is variable in voltage and frequency, connected to the control of the inverter, is state of the art described in IEC and IEEE standards.

3. Over /Under voltage protection (OV/UV)

The protection levels and the disconnection times of the inverter concerning over- and under-voltage shall be determined.

The different protection levels must not impair the LVRT/HVRT requirements of NOGA in the graph below (Figure 1), i.e. the inverter must be able to stay connected to the grid as long as the grid voltage is within area 1. The trip parameters should be chosen in a way that the inverter may trip only if the voltage is in area 2.

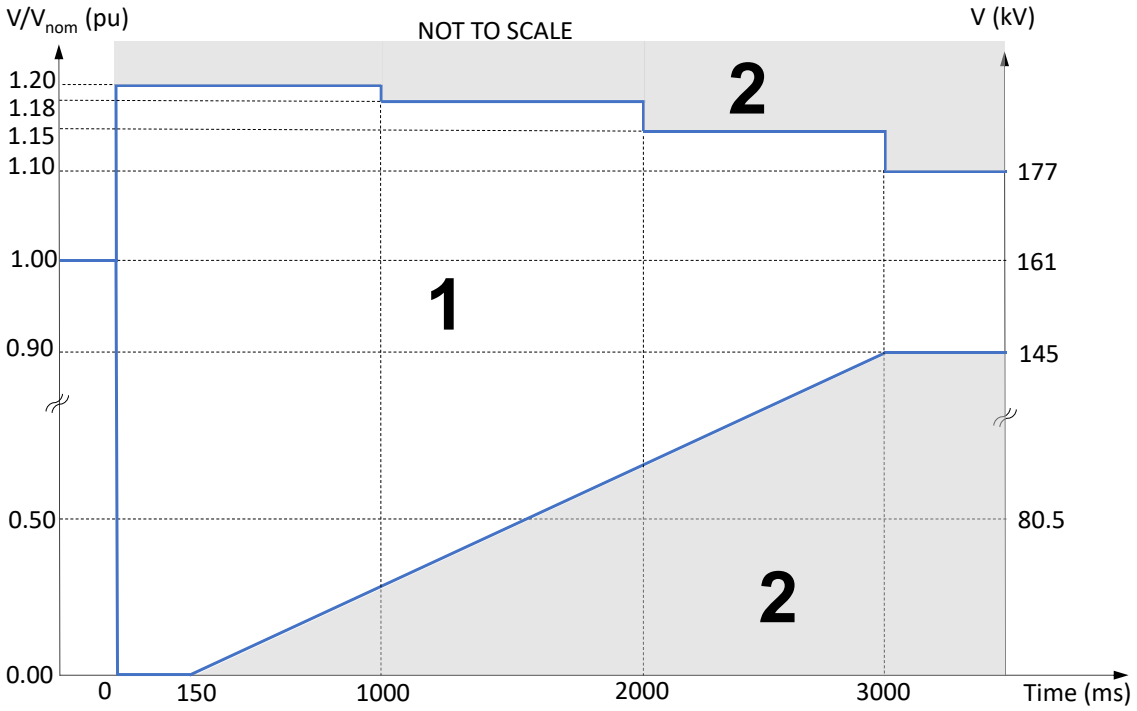

Figure 1: LVRT/HVRT curves

The protection parameters are derived from the requirements above as stated in the following table:

Voltage [% of V_{nom}]	Protection level	Parameter	Trip time setting	Voltage level setting [pu of V_{nom}]
V<50%	Vunder2	VCtl_Lo2Lim	>1750 ms	0.5
50%<V<85%	Vunder1	VCtl_Lo1Lim	>2850 ms	0.85
	Continuous operation			
V>115%	Vover1	VCtl_Hi1Lim	>3000 ms	1.15
V>>130%	Vover2	VCtl_Hi2Lim	>100 ms	1.30

Table 2: Voltage disconnection settings

The following **procedure** shall be applied for the determination of the **under-voltage** protection levels:

1. The voltage of the 3-phase voltage supply shall be decreased from 100 % of nominal voltage in steps of 1% of nominal voltage until the inverter disconnects. Each step shall take at least 10 s.
2. For the determination of the disconnection times the actual trip time measured in step 1 will be evaluated.

The following **procedure** shall be applied for the determination of the **over-voltage** protection levels:

1. The voltage of the 3-phase voltage supply shall be increased from 100 % of nominal voltage in steps of 1% of nominal voltage until the inverter disconnects. Each step shall take at least 10 s.
2. For the determination of the disconnection times the actual trip time measured in step 1 will be evaluated.

4. Reconnection logic

In conjunction with the grid protection functions of the inverter there are two more boundary conditions from the NOGA requirements:

- After disconnection of the inverter (generation facility) from the grid following disturbances, the inverter shall be connected to the system with a delay of 5 minutes, provided that the conditions for synchronization are met.

- The rate of increase of active power after reconnection shall be not more than 10% of the nominal power per minute.

Both functions shall be tested during the OV/UV and/or OF/UF testing procedure for at least one time.

5. FRT (Fault Ride Through) tests

The requirements of the NOGA concerning LVRT and HVRT are shown in Figure 1. The inverter is required not to disconnect due to a voltage drop (charged or discharged or at zero power operation), when the voltage at the facility's connection point is within area 1.

Area 1 in Figure 1:

The Inverter will not be disconnected from the grid and will continue to operate. After the disturbance has been cleared, the Inverter shall return to the active power operation mode before the next disturbance. The response time $T_{Response90\%}$ for a step-type disturbance, which is defined as the time required to reach a value of 90% of the intended value, should not exceed 1 second.

Area 2 in Figure 1:

The Inverter may disconnect for a short time until the disturbance is cleared. After disconnection of the inverter from the grid following disturbances, the inverter shall be reconnected to the system after the synchronization conditions are met, within range of at least 5 minutes.
The rate of increase of active power after reconnection shall be 10% of the nominal power per minute.

If the facility has not been disconnected from the network – after the disturbance has been cleared, the facility shall return to the active power produced before the disturbance. The response time $T_{Response90\%}$ for a step-type disturbance, which is defined as the time required to reach a value of 90% of the planned value, not to exceed one second.

LVRT

Duration of voltage drop	Residual Voltage
> 150 ms	0…5%
> 780 ms	20…30%
> 1570 ms	45…55%
> 2370 ms	70…80%
> 3000 ms	90…100%

Table 3: LVRT Test

HVRT

Duration of voltage drop	Voltage
> 3000 ms	115%
> 2000 ms	118%
> 1000 ms	120%

Table 4: HVRT Test

6. Continuous operation of the inverter between 47 and 53 Hz

The purpose of this type test is to prove the ability of the inverter to operate continuously during abnormal frequencies and rapid frequency changes.

Initial dispatch of ESR is set to the following active power setpoints P_{pre} (with approximately zero reactive power):

P_{pre} (discharge mode) =+0.5pu

P_{pre} (charge mode) =-0.5pu

P_{pre} (ZPO - zero P/Q power operation mode) =0pu

6.1. Continuous operation of the inverter between 47 and 53 Hz with varying voltages

The frequency and voltage of the AC source will be changed following the test sequence in table 5 below. After each step the system must prove stable power output for several seconds (proposed: 20s).

In addition to mentioned above, it will be shown that the operation at varying frequencies is not affected by varying voltages, thus the voltage will vary as outlined in the line below between 60%...112% V_n based on the following table #5.

Step	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
f [Hz]	50	50.1	49.5	48	49	48.5	47.5	47.1	50	50.2	50.7	51.2	52.9	50.7	50.2	50.1	50
Voltage [%V_n]	100	100	95	90	85	80	70	60	80	100	105	110	110	112	105	102	99

Table 5: Voltage and Frequency Cases settings

6.2. Continuous operation of the inverter between 47 and 53 Hz with extreme ROCOF

The frequency of the AC source will be changed following the test sequence in Figure 2.

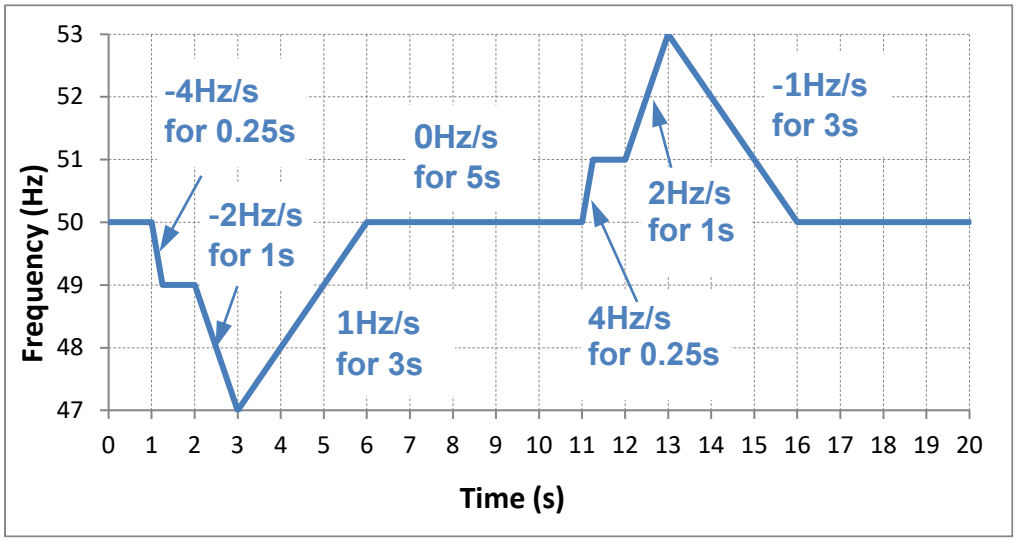

Figure 2: frequency profile with extreme ROCOF

A. The time frame calculation will be pre-defined by Inverter supplier before performing the test.

Results verification:

B. The inverter should remain connected through the test sequence.
C. Inverter active and reactive power output should be well controlled. System frequency and voltage should not oscillate excessively or deviate from steady state levels for any significant time frame.
D. Any oscillation shall be adequately damped

7. Response to frequency change - verification of P(f):

The purpose of this test is to demonstrate the inverter's capability to control the output power as a function of frequency deviation (inertial response should be disabled) at frequency values above and under a certain level.

1. The Inverter will have the ability to control the active power in any operating mode (Charging, Discharging or Zero Power Operation) based on the primary frequency response (in a resolution of -/+ 0.01 Hz or less).
2. The test will demonstrate the ability to operate in the following two regimes:
   A. Limited Frequency Sensitive Mode (**LFSM**) Operating Regime
   B. Frequency Sensitive Mode (**FSM**) Operating Regime

7.1 Inverter regulation in the LFSM (Limited Frequency Sensitive Mode) operating regime:

1. Within the frequency range of 47Hz to 53 Hz (47<f<53 Hz), the inverter will function stably and will adjust the active power (discharged /charged) based on system frequency deviation in any operating mode (Charging, Discharging, Zero Power Operation).
2. Zero Power Operation – When the Inverter is synchronized to the grid and $P_{setpoint}$=0, it is required to respond according to its available capacity.
3. In the frequency range of $[(50 - DB_{UF}) < f < (50+DB_{OF})]$ the Inverter will generate or charge at power as determined during the test $P_{setpoint}$
4. When the frequency increases, the inverter will decrease the active discharging power or increase the active charging power.
5. When the frequency decreases, the inverter will increase the active discharging power or decrease the active charging power.
6. If the Inverter is charging and the frequency decreases, and the Inverter cannot reduce more the charging power, the Inverter will enable change of state from charging to discharging, continuously and without a delay .If the Inverter is discharging and the frequency increases, and the Inverter cannot increase more the discharging power, the Inverter will enable change of state from discharging to charging, continuously and

without a delay. If the inverter is in Zero Power Operation and the frequency decreases or increases the Inverter will enable discharge or charging without a delay.

7. In cases of frequency Increase above 50Hz+DB_{OF} (OF – Over-Frequency), the Inverter will decrease the active power injected to the grid according to the following formula:

$$P = \max\left\{P_{min}\,, P_{pre} + min\left(0, \frac{f_{nom} - f + DB_{OF}}{f_{nom} \times R_{OF}}\right)\right\}$$

8. In cases of a frequency drop below 50Hz-DB_{UF} (UF - Under-Frequency), the Inverter will Increase the active power transmitted to the network according to the following formula:

$$P = \min\left\{P_{avl}\,, P_{pre} + max\left(0, \frac{f_{nom} - f - DB_{UF}}{f_{nom} \times R_{UF}}\right)\right\}$$

Where:

f–actual system frequency (Hz)

f_{nom} – nominal frequency (50 Hz)

P – Active power required to be transmitted to the grid, in relative units (p.u.), based on the P_{nom} of the Inverter

P_{nom} – the nominal power of the Inverter (MW)

Note: Technical requirements such as frequency change response are relative to the value of P_{nom}.

P_{pre} – Active power of the Inverter before disturbance, p.u. based on the P_{nom} of the Inverter

P_{min} – Minimum power, p.u. based on P_{nom}

Note: Minimum power in a storage facility is negative in charge mode, or "0" when the battery is fully charged (depending on SOC (State of Charge))

P_{avl} – available power, p.u. based on P_{nom}

Note: The available power P_{avl} of the Inverter is defined as the active power that the Inverter can transmit to/from the grid, subject to the availability of the power source, the nominal power P_{nom} or P_{STR} (if available), and the operational status of the equipment.

P_{STR} – Short Term Rating power, p.u. based on P_{nom} for prespecified time period.

DB_{OF}, DB_{UF} – Dead Band values for over-frequency and under-frequency respectively (Hz)

R_{OF}, R_{UF} – Frequency droop for over-frequency and under-frequency respectively (p.u.)

9. The default dead band value is set to:

   DB_{OF} = 0.2 Hz

   DB_{UF} = 0.2 Hz

10. The default frequency droop value of the Inverter is set to 2% (R_{OF}=R_{UF}= 0.02 p.u.) based on the nominal power of the facility.

11. The frequency control of the Inverter is required to operate continuously and immediately without delay or latency.
    The response time $T_{Response}$ 90% for a step-type disturbance, defined as the time required to reach a value of 90% of the requested power value, including the frequency measurement time, should not exceed one second.

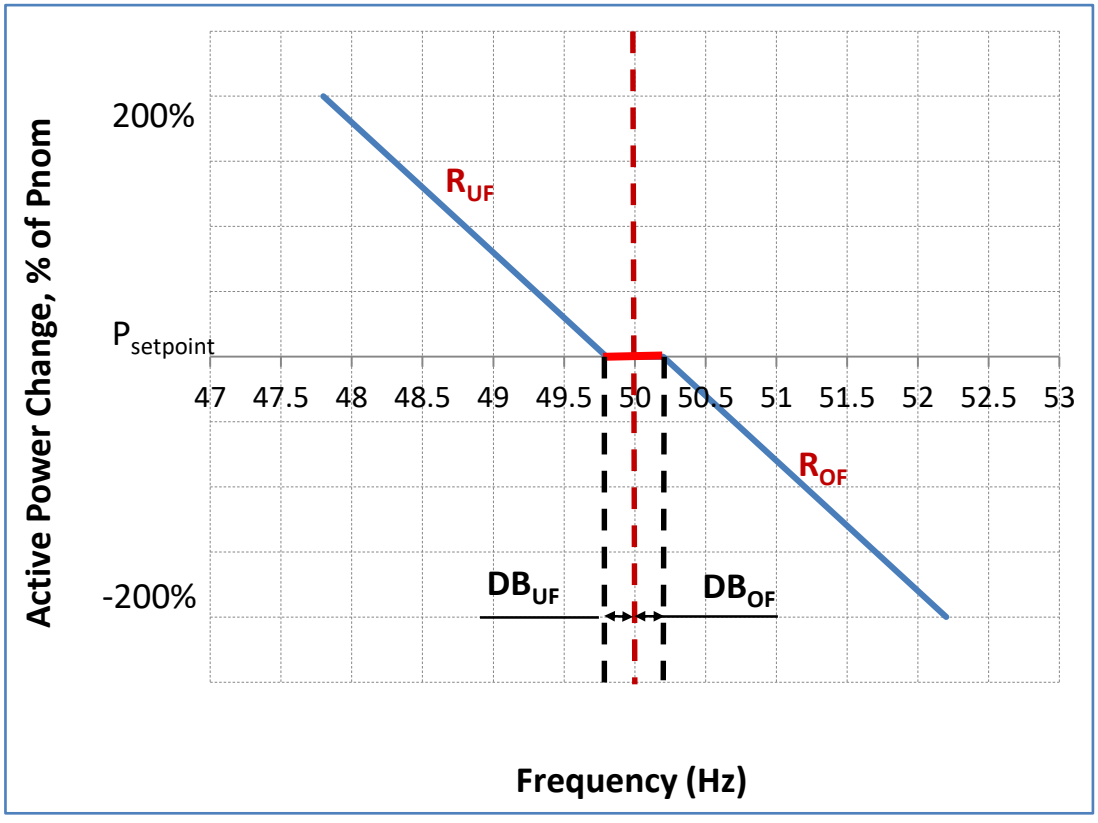

Figure 3: Active power change related to frequency deviation

The following tables provide the test variations:

P_{pre} (discharge mode) =+0.5pu

P_{pre} (charge mode) =-0.5pu

P_{pre} (ZPO - zero P/Q power operation mode) =0pu

$P_{cmd} = P_{pre} + \Delta P$

Where:

P_{cmd} – Committed value of active power required by primary frequency response

ΔP – Change in active power due to frequency deviation Δf

	Initial State	Frequency	Position vs DB	$\Delta P/P_n$ Expected	P_{cmd}/P_n Expected	Cross Zero?	T_{90} Target
1	Discharge	49.8 Hz	At DB edge	~0	+0.50	No	≤ 1 s
2	Discharge	49.5 Hz	Outside DB	+0.30	+0.80	No	≤ 1 s
3	Discharge	49.0 Hz	Outside DB	+0.80	+1.00 (at saturation) (*)	No	≤ 1 s
4	Charge	49.8 Hz	At DB edge	~0	–0.50	No	≤ 1 s
5	Charge	49.5 Hz	Outside DB	+0.30	-0.20	No	≤ 1 s
6	Charge	49.0 Hz	Outside DB	+0.80	+0.30	**Yes** (Charge → Discharge)	≤ 1 s
7	ZPO	49.8 Hz	At DB edge	~0	~0	No	≤ 1 s
8	ZPO	49.5 Hz	Outside DB	+0.30	+0.30	**Yes**, (Zero→Discharge)	≤ 1 s
9	ZPO	49.0 Hz	Outside DB	+0.80	+0.80	**Yes**, (Zero→Discharge)	≤ 1 s
10	Discharge	50.2 Hz	At DB edge	~0	+0.50	No	≤ 1 s
11	Discharge	50.5 Hz	Outside DB	–0.30	+0.20	No	≤ 1 s
12	Discharge	51.0 Hz	Outside DB	–0.80	–0.30	**Yes** (Discharge → Charge)	≤ 1 s
13	Charge	50.2 Hz	At DB edge	~0	–0.50	No	≤ 1 s
14	Charge	50.5 Hz	Outside DB	–0.30	–0.80	No	≤ 1 s
15	Charge	51.0 Hz	Outside DB	–0.80	–1.00 (at saturation) (*)	No	≤ 1 s
16	ZPO	50.2 Hz	At DB edge	~0	~0	No	≤ 1 s
17	ZPO	50.5 Hz	Outside DB	-0.30	-0.30	**Yes**, (Zero→charge)	≤ 1 s

	Initial State	Frequency	Position vs DB	$\Delta P/P_n$ Expected	P_{cmd}/P_n Expected	Cross Zero?	T_{90} Target
18	ZPO	51.0 Hz	Outside DB	-0.80	-0.80	**Yes**, (Zero→charge)	≤ 1 s

(*) or ±1.3 if enabled by P_{STR}

Table 6: Under and over frequency tests in LFSM regime

7.2 Inverter Regulation in a Frequency Sensitive Mode (FSM) operating regime:

In an FSM operating regime, the inverter will allow a continuous response to the change of frequency (dead band=0).

ID	Initial State	Frequency	$\Delta P/P_n$ Expected	Pcmd/Pn Expected	Cross Zero?	T90 Target
1	Discharge	49.8 Hz	+0.20	+0.70	No	≤ 1 s
2	Discharge	49.5 Hz	+0.50	+1.00	No	≤ 1 s
3	Discharge	49.0 Hz	+1.00	+1.00 (at saturation)(*)	No	≤ 1 s
4	Charge	49.8 Hz	+0.20	–0.30	No	≤ 1 s
5	Charge	49.5 Hz	+0.50	0.00	**Yes**, (Charge→Zero)	≤ 1 s
6	Charge	49.0 Hz	+1.00	+0.50	**Yes**, (Charge→Discharge)	≤ 1 s
7	ZPO	49.8 Hz	+0.20	+0.20	**Yes**, (Zero→Discharge)	≤ 1 s
8	ZPO	49.5 Hz	+0.50	+0.50	**Yes**, (Zero→Discharge)	≤ 1 s
9	ZPO	49.0 Hz	+1.00	+1.00	**Yes**, (Zero→Discharge)	≤ 1 s
10	Discharge	50.2 Hz	–0.20	+0.30	No	≤ 1 s
11	Discharge	50.5 Hz	–0.50	0.00	**Yes**, (Discharge→Zero)	≤ 1 s
12	Discharge	51.0 Hz	–1.00	–0.50	**Yes**, (Discharge→Charge)	≤ 1 s
13	Charge	50.2 Hz	–0.20	–0.70	No	≤ 1 s
14	Charge	50.5 Hz	–0.50	–1.00	No	≤ 1 s
15	Charge	51.0 Hz	–1.00	–1.00 (at saturation)(*)	No	≤ 1 s

ID	Initial State	Frequency	ΔP/P_n Expected	Pcmd/Pn Expected	Cross Zero?	T90 Target
16	ZPO	50.2 Hz	–0.20	-0.20	**Yes**, (Zero→charge)	≤ 1 s
17	ZPO	50.5 Hz	–0.50	-0.50	**Yes**, (Zero→charge)	≤ 1 s
18	ZPO	51.0 Hz	–1.00	–1.00	**Yes**, (Zero→charge)	≤ 1 s

(*) or according to P_{STR}

Table 7: Under and over frequency tests in FSM regime

8. Voltage Amplitude response – Grid Forming - capability test

The Grid Forming (Amplitude response) tests should demonstrate the inverter's capability to maintain and form the frequency and voltage between pre-defined limits

In voltage response test, a step change is applied to the voltage value of the voltage source, so that the reactive power response time and value can be measured (Figure 4). The purpose of this test is to demonstrate the capability to respond to voltage Amplitude change as per capability to inject / absorb reactive power.

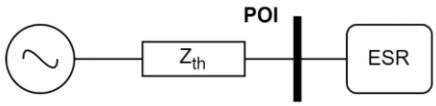

Figure 4: Testbench single-machine variable impedance system

Testbench Setup:

Set the impedance of Z_{th} as close to zero.

Initial dispatch of Energy Storage Resource (ESR) is set to the max discharging for active power with approximately zero reactive power.

Test Sequence (Figure 5):

1. The value of the voltage source behind the equivalent grid impedance decreased instantaneously by 3% (i.e., from 1.0 pu to 0.97 pu)
2. 5 seconds later, the value of voltage source is increased by 3% to return to 1.0 pu
3. 5 seconds later, the value of voltage source is increased by 3% to reach 1.03 pu
4. 5 seconds later, the value of voltage source decreased by 3% to return to 1.0 pu

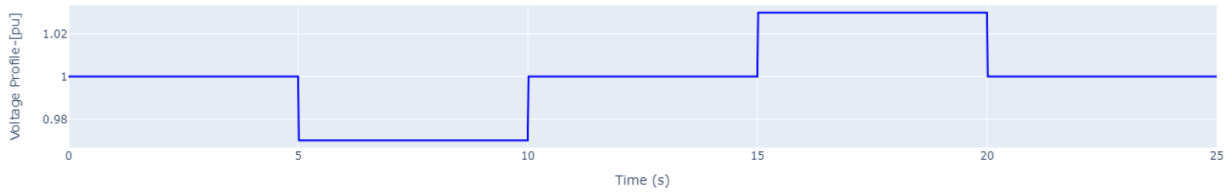

Figure 5: voltage amplitude response test sequence

Results verification:

A. Instantaneous reactive power output of the inverter should quickly respond to opposite voltage step change for each of the 3% voltage step changes, with an initial peak reactive power change of at least 0.03 p.u. on the rated power base (e.g., a 100 MVA rated plant with 0 MVAR initial output should instantaneously increase reactive power output from 0 MVAr to at least 3 MVAr when source voltage magnitude is decreased by 3%.)
   Note: Reactive power should be kept at pre disturbance level for at least for 6 cycles.
B. Response time of 90% of initial change in instantaneous reactive power should occur within 1 cycle.
C. Any oscillation should be damp.
D. The final reactive power after each 3% step change is expected to reach the maximum reactive capability of the inverter to regulate the original voltage set point at 1.0 pu.

9. Active Phase Jump Power – Grid Forming - capability test

This test applies to the phase angle step change to the 3-phase voltage source. As result the active power response time and its value are measured according to the testbench in Figure 4.

This test is set up to examine:

1) The capability to maintain the voltage phasor and resist angle change.
2) Steady state behavior under different angle step changes when it is operating close to the maximum current limit.

For large angle changes forcing the controls beyond their maximum current limits, the ESR should be stable and should not degrade the performance of the power grid.

Testbench Setup:

SCR (Short Circuit Ratio) at connection point is set to 3, system equivalent X/R ratio is set to 6.

Initial dispatch of ESR is set to 50% of the active power (discharge mode) with approximately zero reactive power.

Test Sequence (Figure 6):

1. Angle of the voltage source behind the equivalent grid impedance is decreased instantaneously by 10 degrees.
2. 10 seconds later, angle of voltage source is increased by 10 degrees.
3. 10 seconds later, angle of voltage source decreases instantaneously by 30 degrees.
4. 10 seconds later, angle of voltage source is increased by 30 degrees.
5. 10 seconds later, angle of voltage source decreased instantaneously by 60 degrees.
6. 10 seconds later, angle of voltage source is increased by 60 degrees.

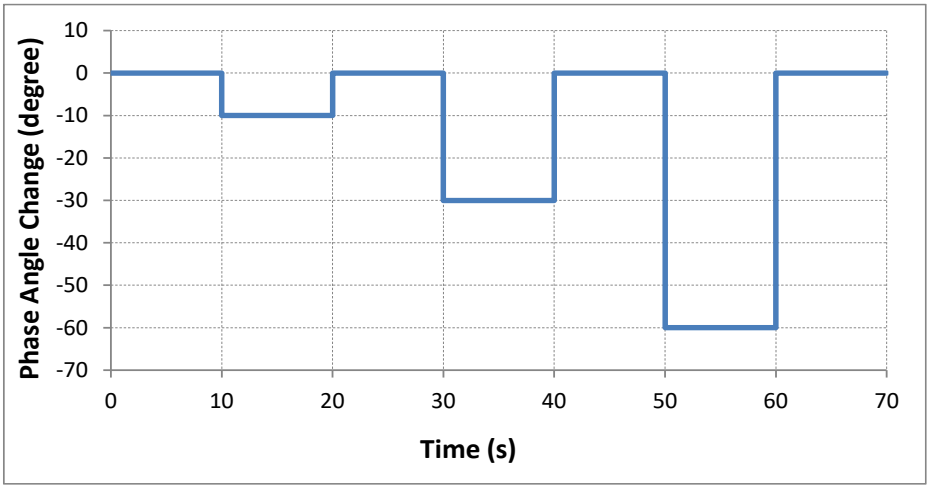

Figure 6: Active phase jump power test sequence

Results verification:

A. Instantaneous active power output of the inverter should quickly respond to oppose the angle change for each of the degree voltage phase angle jumps, with a peak active power change of at least 0.2 pu on the rated active power base (e.g. a 100 MW rated plant should temporarily increase active power output from 50 MW to at least 70 MW when source voltage angle is decreased by 10 degrees, and should temporarily decrease active power from 50 to 30 MW or below when voltage source angle is increased by 10 degrees).

B. For each of the degree voltage phase angle change, response time to 90% of initial

change in instantaneous active power should occur within 15ms.

C. Active power settles to pre-disturbance level shortly after all phase change.

D. If active power / current reaches limits for the 60-degree phase change, the inverter should return to pre-event power levels in a stable manner.

E. Any oscillation should be damp.

F. Any distortion observed in phase quantities should dissipate over time.

10. Low SCR operation - Grid Forming - capability test

This test shall demonstrate ESR stable response for all tested SCR (Short Circuit Ratio) values from 10 to 1.25 according to the testbench in Figure 7.

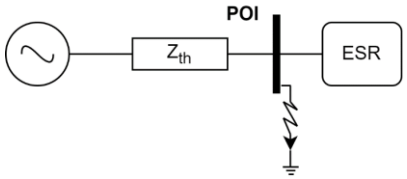

Figure 7: Testbench single-machine variable impedance system for SCR test

Testbench Setup:

Initial SCR at connection point is set to 10. System Equivalent X/R is set to 6.

Initial dispatch of ESR is set to the maximum discharging for active power with approximately zero reactive power.

Test Sequence (Figure 8):

SCR at connection point stepped down repeatedly in this progression: 10, 5, 3, 1.5, 1.25

A 2-phase to ground, 6-cycle fault is applied just before each SCR transition.

The SCR transition occurs at fault clearing time.

The time between faults is 5 seconds.

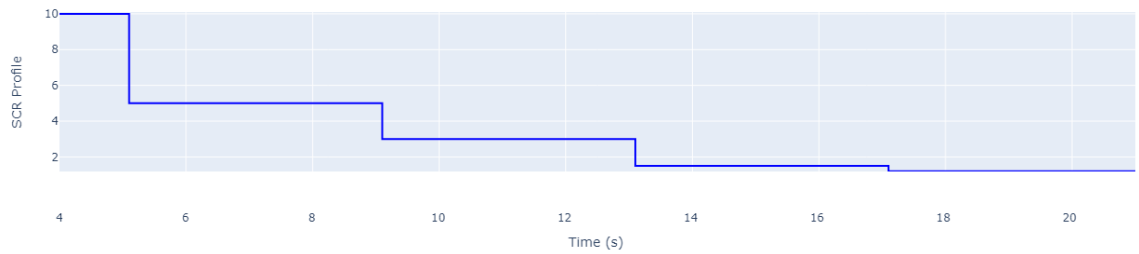

Figure 8: Short circuit ratio test sequence

Results verification:

ESR active and reactive power output and RMS voltage should be well controlled, and ESR should not trip nor reduce power or voltage (except of the fault period) for any extended period down for all tested SCR range from 10 to 1.25.

Any oscillation shall be damped.

11. Active ROCOF Response Power – Grid Forming - capability test

This test demonstrates the Active Power Inertia generated by a Grid Forming inverter as a response to a rate of change of the System Frequency (ROCOF).

For this dedicated test, the active power control as function of frequency deviation should be disabled.

Testbench Setup:

Using Testbench shown in Figure 4, SCR at connection point is set to 3. System Equivalent X/R is set to 6.

Apply the frequency profile shown in Figure 9 to the controllable voltage source of the Testbench. The frequency changes down from 50 Hz to 49 Hz by ROCOF of 1 Hz/s. The frequency stays for 5 seconds at 49 Hz and then returns to the 50 Hz by the same ROCOF and stays at 50 Hz until the active output power reaches steady state (for example 5 seconds). Then the frequency increases from 50 Hz to 51 Hz by ROCOF of 1 Hz/s. The frequency stays for 5 seconds at 51 Hz and then returns to the 50 Hz by the same ROCOF and stays at 50 Hz until the output power reaches steady state (for example 5 seconds).

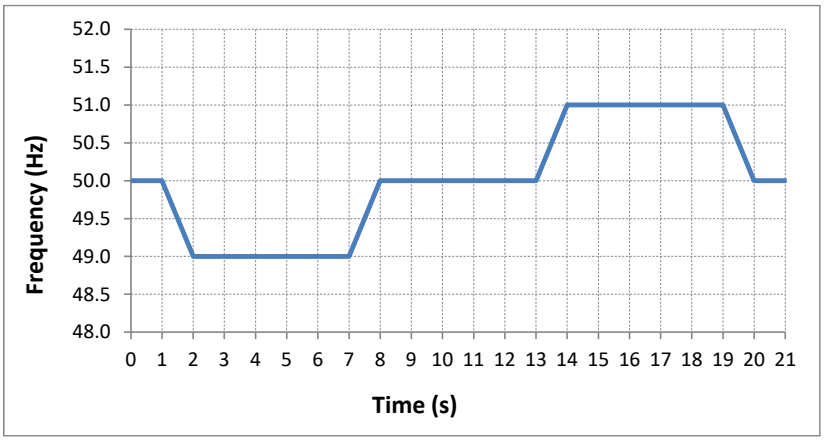

Figure 9: Frequency profile for inertia test sequence

The following table provides the test variations:

	Initial State	Frequency	ROCOF	$\Delta P/P_n$ Expected	P_{cmd}/P_n Expected	T_{90} Target
1	Discharge	50 Hz	0	0	+0.50	
2	Discharge	50→49 Hz	-1 Hz/s	+0.20	+0.70	≤ 300ms
3	Discharge	49 Hz	0	0	+0.50	≤ 300ms
4	Discharge	49→50 Hz	+1 Hz/s	-0.2	+0.3	≤ 300ms
5	Discharge	50 Hz	0	0	+0.50	≤ 300ms
6	Discharge	50→51 Hz	+1 Hz/s	-0.2	+0.3	≤ 300ms
7	Discharge	51 Hz	0	0	+0.50	≤ 300ms
8	Discharge	51→50 Hz	-1 Hz/s	+0.20	+0.70	≤ 300ms
9	Discharge	50 Hz	0	0	+0.50	≤ 300ms
10	Charge	50 Hz	0	0	-0.50	
11	Charge	50→49 Hz	-1 Hz/s	+0.20	-0.30	≤ 300ms
12	Charge	49 Hz	0	0	-0.50	≤ 300ms
13	Charge	49→50 Hz	+1 Hz/s	-0.2	-0.7	≤ 300ms
14	Charge	50 Hz	0	0	-0.50	≤ 300ms
15	Charge	50→51 Hz	+1 Hz/s	-0.2	-0.7	≤ 300ms
16	Charge	51 Hz	0	0	-0.50	≤ 300ms
17	Charge	51→50 Hz	-1 Hz/s	+0.20	-0.30	≤ 300ms
18	Charge	50 Hz	0	0	-0.50	≤ 300ms
19	ZPO	50 Hz	0	0	0	
20	ZPO	50→49 Hz	-1 Hz/s	+0.20	+0.20	≤ 300ms
21	ZPO	49 Hz	0	0	0	≤ 300ms
22	ZPO	49→50 Hz	+1 Hz/s	-0.2	-0.2	≤ 300ms
23	ZPO	50 Hz	0	0	0	≤ 300ms

	Initial State	Frequency	ROCOF	$\Delta P/P_n$ Expected	P_{cmd}/P_n Expected	T_{90} Target
24	ZPO	50→51 Hz	+1 Hz/s	-0.2	-0.2	≤ 300ms
25	ZPO	51 Hz	0	0	0	≤ 300ms
26	ZPO	51→50 Hz	-1 Hz/s	+0.20	+0.20	≤ 300ms
27	ZPO	50 Hz	0	0	0	≤ 300ms

Table 8: ROCOF Response test

Initial dispatch of ESR is set to the following active power setpoints P_{pre} (with approximately zero reactive power):

P_{pre} (discharge mode) =+0.5pu

P_{pre} (charge mode) =-0.5pu

P_{pre} (ZPO-zero P/Q power operation mode) =0pu

$P_{cmd} = P_{pre} + \Delta P$

In this test: ΔP - Change in active power due to ROCOF

Results verification:

A. Inverters' active and reactive power output should be well controlled. System frequency and voltage should not oscillate excessively or deviate from steady state levels for any significant amount of time.
B. Voltage settles to a stable operating point when frequency is not ramping.
C. Active power should behave according to the ROCOF, with K_{ROCOF}=0.2, when frequency is ramping.
D. Any oscillation shall be adequately damped.

12. Black start – Grid Forming - capability test

The ability of the inverter to provide Black Start capability, i.e. to energize a dead bus without any external voltage or frequency source.

Verify that the inverter may energize a dead bus (Figure 10) and keep the nominal voltage & frequency.

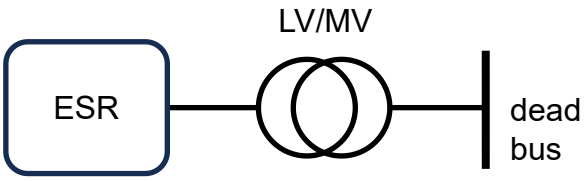

Figure 10: Black start tests system example